CLAIMS

What is claimed is:

1. A combination of static random access memory (SRAM) and mask read only memory (MROM) cells, including a SRAM unit and a ROM unit, wherein the static random access unit as a random access memory unit comprises a first transistor, a second transistor, a third transistor, a fourth transistor, a fifth transistor, and a sixth transistor; the first transistor, the second transistor, the third transistor, and the fourth transistor forming an inverter; the first transistor being complementary to the third transistor, the second transistor being complementary to the fourth transistor, which is characterized in that:

the ROM unit being a MROM is used to permanently store data and has a seventh transistor, with the feature that the ROM unit is embedded inside the SRAM unit.

2. The memory cell combination of claim 1, wherein the first transistor, the second transistor, the third transistor, the fourth transistor, the fifth transistor, the sixth transistor, and the seventh transistor are metal oxide semiconductor field effect transistors (MOSFET's).

3. The memory cell combination of claim 1, wherein the ROM unit is in the cross region formed by the intersection of the polysilicon area and a source Vss of the fifth transistor and the sixth transistor with the ROM bit line contact next to the ROM unit.

4. The memory cell combination of claim 1, wherein the SRAM unit and the ROM unit share the same word line.

5. The memory cell combination of claim 1, wherein the SRAM unit and the ROM unit share the same source (Vss) contact.

6. The memory cell combination of claim 1, wherein the SRAM unit and the ROM

unit share the same X-decoder circuit.

7. A combination of static random access memory (SRAM) and mask read only memory (MROM) cells, including a SRAM unit and a ROM unit, wherein the static random access unit as a random access memory unit comprises a first transistor, a second transistor, a third transistor, a fourth transistor, a fifth transistor, and a sixth transistor; the first transistor, the second transistor, the third transistor, and the fourth transistor forming an inverter; the first transistor being complementary to the third transistor, the second transistor being complementary to the fourth transistor, which is characterized in that:

the ROM unit being a MROM is used to permanently store data and has a seventh transistor, with the feature that the ROM unit is formed in the cross region formed at the intersection of the active area extension where the polysilicon area and a source contact of the fifth transistor and the sixth transistor are located, so that the ROM unit is embedded inside the SRAM unit.

8. The memory cell combination of claim 7, wherein the ROM bit line contact next to the ROM unit.

9. The memory cell combination of claim 7, wherein the SRAM unit and the ROM unit share the same word line.

10. The memory cell combination of claim 7, wherein the SRAM unit and the ROM unit share the same source (Vss) contact.

11. The memory cell combination of claim 7, wherein the SRAM unit and the ROM unit share the same X-decoder circuit.

12. A combination of static random access memory (SRAM) and mask read only memory (MROM) cells, comprising:

a static random access unit, which has at least a first transistor, a second transistor, a third transistor, a fourth transistor, a fifth transistor, and a sixth

transistor; wherein the first transistor, the second transistor, the third transistor, and the fourth transistor form an inverter, the first transistor is complementary to the third transistor, and the second transistor is complementary to the fourth transistor;

a read only memory (ROM) unit, which has at least a seventh transistor;

a first bit line, which is connected to the source/drain of the fifth transistor;

a second anti-bit line, which is connected to the source/drain of the sixth transistor;

a third bit line, which is connected to the source/drain of the seventh transistor; and

a word line, which is connected to the gates of the fifth transistor, the sixth transistor and the seventh transistor for controlling the fifth transistor, the sixth transistor and the seventh transistor.

13. The memory cell combination of claim 12, wherein the ROM unit is formed in the cross region formed at the intersection of the active area extension where the polysilicon area and a source contact of the fifth transistor and the sixth transistor are located, so that the ROM unit is embedded inside the SRAM unit.

14. The memory cell combination of claim 12, wherein the ROM unit is a mask read only memory (MROM).

15. The memory cell combination of claim 12, wherein the first transistor, the second transistor, the third transistor, the fourth transistor, the fifth transistor, the sixth transistor, and the seventh transistor are metal oxide semiconductor field effect transistors (MOSFET's).

16. The memory cell combination of claim 12, wherein the ROM bit line contact next

to the ROM unit.

17. The memory cell combination of claim 12, wherein the SRAM unit and the ROM unit share the same word line.

18. The memory cell combination of claim 12, wherein the SRAM unit and the ROM unit share the same source (Vss) contact.

19. The memory cell combination of claim 12, wherein the SRAM unit and the ROM unit share the same X-decoder circuit.